IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A fuse box, comprising:

a plurality of make-links for programming an address of a defective normal memory cell with an address of a corresponding redundant memory cell, wherein the make-links are formed by at least one conductor in a first layer having its elongated axis disposed at a substantially perpendicular angle relative to at least one conductor in a second layer.

2. (Original) The fuse box of claim 1, wherein the address of the defective normal memory cell and the address of the corresponding redundant memory cell are row addresses or column addresses.

3. (Currently Amended) A fuse box as defined in Claim 1, where the plurality of make-links are disposed to replace ~~comprising:~~

~~a plurality of make-links for replacing~~ a defective normal bit line with a corresponding redundant bit line.

4. (Currently Amended) A fuse box as defined in Claim 1, where the plurality of make-links are disposed to replace~~comprising~~

~~a plurality of make-links for replacing~~ a defective normal word line with a corresponding redundant word line.

5. (Currently Amended) A redundant address decoder, comprising:

a fuse box including a plurality of make-links for decoding an address of a defect cell, where each of the make-links includes a first end and a second end; ~~and~~

a redundant word line selection circuit for selecting a word line of a redundant cell corresponding to the address of the defect cell in response to a signal output from the fuse box;

a redundancy enable signal line;

a plurality of transistors, each of the plurality of transistors having a source connected to the first end of one of the plurality of make-links and a gate connected to said redundancy enable signal line; and

a plurality of nodes, each of the plurality of nodes connected to the second end of one of the plurality of make-links.

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Currently amended) The redundancy address decoder of ~~claim 8~~Claim 5, further comprising another plurality of nodes for receiving defect cell addresses, wherein each of the plurality of transistors has a drain connected to one of the other plurality of nodes.

10. (Currently Amended) A redundant address decoder, comprising:

a fuse box including a plurality of make-links for decoding an address of a defect cell, where each of the make-links includes a first end and a second end; ~~and~~

a redundant bit line selection circuit for selecting a bit line of a redundant cell corresponding to the address of the defect cell in response to a signal output from the fuse box;

a redundancy enable signal line;

a plurality of transistors, each of the plurality of transistors having a source connected to the first end of one of the plurality of make-links and a gate connected to said redundancy enable signal line; and

a plurality of nodes, each of the plurality of nodes connected to the second end of one of the plurality of make-links.

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Currently Amended) The redundancy address decoder of ~~claim 13~~Claim 10, further comprising another plurality of nodes for receiving defect cell addresses, wherein each of the plurality of transistors has a drain connected to one of the other plurality of nodes.

15. (Currently Amended) A method for repairing a defective memory cell, comprising the steps of:

receiving an address of the defective cell;

decoding the address of the defective cell through make-links, wherein the make-links are formed by at least one conductor in a first layer having its elongated axis disposed at a substantially perpendicular angle relative to at least one conductor in a second layer; and

selecting a redundant word line corresponding to the address of the defective cell and replacing the defective cell with a redundant cell.

16. (NEW) A redundant address decoder, comprising:

a fuse box including a plurality of make-links for decoding an address of a defect cell, where each of the make-links includes a first end and a second end;

a plurality of transistors, each of the plurality of transistors having a source connected to the first end of one of the plurality of make-links, respectively;

a plurality of nodes, each of the plurality of nodes connected to the second end of one of the plurality of make-links, respectively; and

a redundant word line selection circuit for selecting a word line of a redundant cell corresponding to the address of the defect cell in response to a signal output from the fuse box, wherein the redundant word line selection circuit includes an inverter connected to a first one of the plurality of nodes for performing an inversion operation, a first NAND gate connected to second and third ones of the plurality of nodes for performing a NAND operation, a second NAND gate connected to fourth and fifth ones of the plurality

of nodes for performing the NAND operation, and a NOR gate connected to the inverter as well as both the first and second NAND gates for performing a NOR operation.

17. (NEW) The redundancy address decoder of claim 16, wherein each of the plurality of transistors have a gate connected to a redundancy enable signal line.

18. (NEW) The redundancy address decoder of claim 17, further comprising another plurality of nodes for receiving defect cell addresses, wherein each of the plurality of transistors has a drain connected to one of the other plurality of nodes.

19 (NEW) A redundant address decoder, comprising:

a fuse box including a plurality of make-links for decoding an address of a defect cell, where each of the make-links includes a first end and a second end; and

a plurality of transistors, each of the plurality of transistors having a source connected to the first end of one of the plurality of make-links, respectively;

a plurality of nodes, each of the plurality of nodes connected to the second end of one of the plurality of make-links, respectively; and

a redundant word line selection circuit for selecting a word line of a redundant cell corresponding to the address of the defect cell in response to a signal output from the fuse box, wherein the redundant word line selection circuit includes an inverter connected to a first one of the plurality of nodes for performing an inversion operation, a first NAND gate connected to second and third ones of the plurality of nodes for performing a NAND operation, a second NAND gate connected to fourth and fifth ones of the plurality

of nodes for performing the NAND operation, and a NOR gate connected to the inverter as well as both the first and second NAND gates for performing a NOR operation.

20. (NEW) The redundancy address decoder of claim 19, wherein each of the plurality of transistors have a gate connected to a redundancy enable signal line.

21. (NEW) The redundancy address decoder of claim 20, further comprising another plurality of nodes for receiving defect cell addresses, wherein each of the plurality of transistors has a drain connected to one of the other plurality of nodes.